In the Claims:

1. (Previously Presented) A transistor, comprising:

a workpiece;

a doped region disposed in the workpiece, the doped region including a dopant species;

a doped gate dielectric disposed over the doped region of the workpiece, the doped gate dielectric including the dopant species, wherein the doped gate dielectric comprises about 50 Å or less of Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, TiO_2, $HfSiO_x$, ZrO_2, or $ZrSiO_x$;

a gate disposed over the gate dielectric; and

a source region and a drain region formed in at least the doped region of the workpiece, wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.

2. (Original) The transistor according to Claim 1, wherein the dopant species comprises at least one Group V, VI or VII element.

3. (Previously Presented) The transistor according to Claim 2, wherein the dopant species comprises fluorine.

4. (Original) The transistor according to Claim 1, wherein the doped region comprises a thickness of about 100 Å or less.

5. (Original) The transistor according to Claim 1, wherein the dopant species fills vacancies in the atomic structure of the gate dielectric.

6. (Previously Presented) The transistor according to Claim 1, wherein the doped gate dielectric comprises a high k dielectric material.

7. (Canceled)

8. (Original) The transistor according to Claim 1, further comprising a thin insulating layer disposed between the gate dielectric and the doped region of the workpiece.

9. (Original) The transistor according to Claim 8, wherein the thin insulating layer comprises a thickness of about 10 Å or less.

10. (Original) The transistor according to Claim 9, wherein the thin insulating layer comprises silicon dioxide or silicon oxynitride.

11. (Original) The transistor according to Claim 1, wherein the workpiece comprises a silicon-on-insulator (SOI) wafer.

12-36. (Canceled)

37. (Previously Presented) The transistor according to Claim 2, wherein the dopant species comprises nitrogen.

38. (Previously Presented) The transistor according to Claim 1, wherein the doped gate dielectric comprises an oxide.

39. (Previously Presented) The transistor according to Claim 1, wherein the gate comprises a semiconductor material.

40. (Previously Presented) The transistor according to Claim 1, wherein the gate comprises a metal.

41. (Currently Amended) A transistor, comprising:

a workpiece;

a doped region disposed in the workpiece, the doped region including a dopant species, wherein the dopant species comprises fluorine;

a doped gate dielectric disposed over the doped region of the workpiece, the doped gate dielectric including the dopant species;

a metal gate disposed over the gate dielectric; and

a source region and a drain region formed in at least the doped region of the workpiece, wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.

42. (Currently Amended) The transistor according to Claim [[41]] 46, wherein the dopant species comprises at least one Group V, VI or VII element.

43. (Currently Amended) The transistor according to Claim [[42]] 46, wherein the dopant species comprises fluorine.

44. (Previously Presented) The transistor according to Claim 42, wherein the dopant species comprises nitrogen.

45. (Previously Presented) The transistor according to Claim 41, wherein the doped gate dielectric comprises a high k dielectric material.

46. (Currently Amended) [[The]] A transistor, comprising: ~~according to Claim 45,~~

a workpiece;

a doped region disposed in the workpiece, the doped region including a dopant species;

a doped gate dielectric disposed over the doped region of the workpiece, the doped gate dielectric including the dopant species, wherein the doped gate dielectric comprises about 50 Å or less of Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, TiO_2, $HfSiO_x$, ZrO_2, or $ZrSiO_x$;

a metal gate disposed over the gate dielectric; and

a source region and a drain region formed in at least the doped region of the workpiece, wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.

47. (Previously Presented) The transistor according to Claim 41, further comprising a thin insulating layer disposed between the gate dielectric and the doped region of the workpiece, wherein the thin insulating layer comprises a thickness of about 10 Å or less.

48. (Previously Presented) The transistor according to Claim 44, wherein the thin insulating layer comprises silicon dioxide.

49. (Previously Presented) The transistor according to Claim 44, wherein the thin insulating layer comprises silicon oxynitride.

50. (Previously Presented) The transistor according to Claim 41, wherein the workpiece comprises a silicon-on-insulator (SOI) wafer.

51. (Previously Presented) The transistor according to Claim 41, wherein the doped gate dielectric comprises an oxide.

52. (Previously Presented) The transistor according to Claim 41, wherein the gate comprises a semiconductor material.

53. (Previously Presented) The transistor according to Claim 41, wherein the gate comprises a metal.